AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-19. (Canceled)

20. (New) A wide multiplexer to multiplex multiple bits with minimal time delay comprising:

a first passgate circuit coupled to receive a first plurality of input bits and a first plurality of select signals, the first plurality of select signals to select which corresponding one of the first plurality of input bits is passed through a passgate and onto a first node;

a first default circuit also coupled to receive the first plurality of select signals and to output a first default voltage onto the first node, if the first plurality of select signals select none of the first plurality of input bits through to the first node;

a second passgate circuit coupled to receive a second plurality of input bits and a second plurality of select signals, the second plurality of select signals to select which corresponding one of the second plurality of input bits is passed through a passgate and onto a second node; and

a second default circuit also coupled to receive the second plurality of select signals and to output a second default voltage onto the second node, if the second plurality of select signals select none of the second plurality of input bits through to the second node; and

an output logic gate coupled directly to the first and second nodes to receive either one of the selected first plurality of inputs bits or the first default voltage directly as a first gate input and either one of the selected second plurality of inputs or the second default voltage directly as a second gate input and in response to generate an output from the output logic gate with minimal time delay in response to a wide bit-width input to the wide multiplexer.

21. (New) The wide multiplexer as recited in claim 20, wherein the first default circuit includes a first OR gate to receive the first plurality of select signals and to drive a first transistor to place the first default voltage onto the first node if none of the first plurality of input bits is passed through to the first node; and wherein the second default circuit includes a second OR gate to receive the second plurality of select signals and to drive a second transistor to place the second default voltage onto the second node if none of the second plurality of input bits is passed through to the second node.

22. (New) The wide multiplexer as recited in claim 21, wherein the output logic gate is a NAND gate.

23. (New) The wide multiplexer as recited in claim 20, wherein the first default circuit includes a first NOR gate to receive the first plurality of select signals and to drive a first transistor to place the first default voltage onto the first node if none of the first plurality of input bits is passed through to the first node; and wherein the second default circuit includes a second NOR gate to receive the second plurality of select signals and to drive a second transistor to place the second default voltage onto the second node if none of the second plurality of input bits is passed through to the second node.

24. (New) The wide multiplexer as recited in claim 23, wherein the output logic gate is a NOR gate.

25. (New) The wide multiplexer as recited in claim 20 further comprising a third passgate circuit coupled to receive a third plurality of input bits and a third plurality of select signals, the third plurality of select signals to select which corresponding one of the third plurality of input bits is passed through a passgate and onto a third node;

a third default circuit also coupled to receive the third plurality of select signals and to output a third default voltage onto the third node, if the third plurality of select signals select none of the third plurality of input bits through to the third node;

the output logic gate also coupled directly to the third node to receive either one of the selected third plurality of inputs bits or the third default voltage directly as a third

gate input in response to inputs from the first, second and third nodes to generate the output from the output logic gate with minimal time delay.